Power Tile: Objectives and Program Status

California Institute of Technology

- **Objectives:**
  - Develop a modular solar power harvesting and storage system with at least a 20% decrease in mass/kW delivered continuously .

- **Innovation:**

  The power tile is enabled by the synergistic combination of novel technologies: ultra-long life inorganic solid state Li batteries, thin-film nanowire based thermoelectric devices, integrated power management.

- **Program Status:**
  - Project inception, July 2001
  - 3 Generations of prototype power tile created
    - Proof of concept achieved
    - Thermoelectric layer found to increase device efficiency by at least 5%
    - Functional PMAD circuit

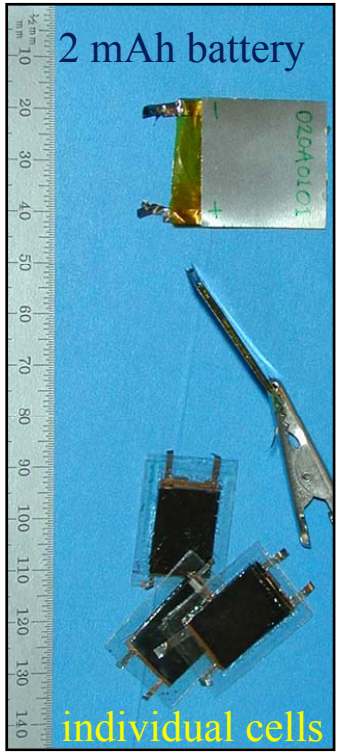
task manager: Jay Whitacre

Power Tile: Major Accomplishments

California Institute of Technology

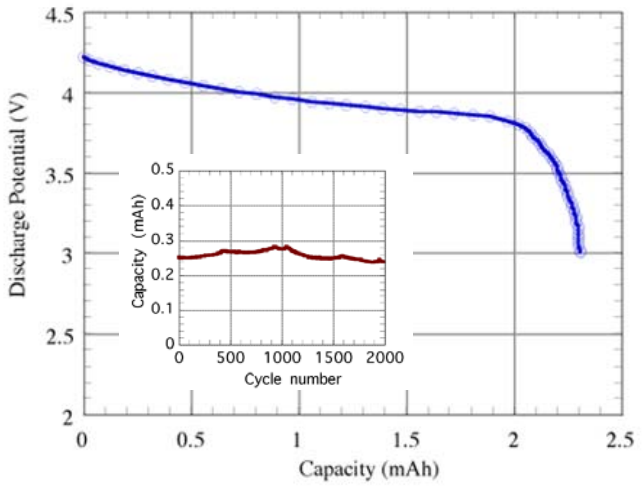
Battery fabrication/testing

- Partnership with Front Edge technologies created to produce multilayer thin film batteries
- Packaged, high capacity cells produced, delivered, tested - excellent temperature and lifetime performance demonstrated.



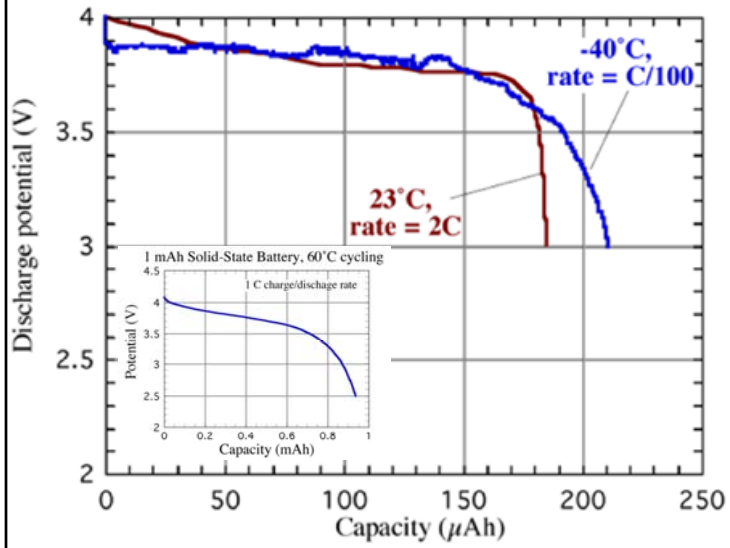
Cells packaged in Stainless Steel

Performance



- Capacities approaching 2.5 mAh/cm^2
- Over 2000 full charge/discharge cycles displayed with no significant capacity fade
- Li-based solid state chemistry - 3.9 V discharge

Temperature testing



- Functional at -40 ˚C
- Must use low-current discharge rate
- Fully functional up to 65˚ C - 5C discharge rate possible

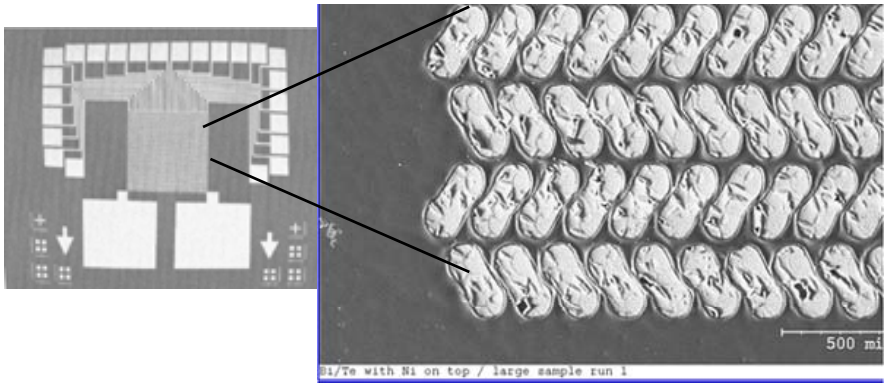
task manager: Jay Whitacre

Power Tile: Major Accomplishments

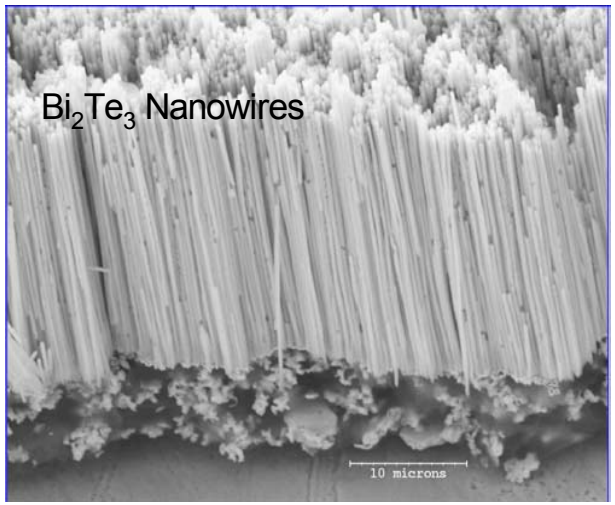
Thin film thermoelectric device

- Functional thin film microdevice recently demonstrated by JPL thermoelectric device technologies group

- Development of nanowire template patterning process achieved
  - Allows for the the fabrication of nanowire-based thermoelectric devices



SEM image showing microdevice elements as developed under DOD funding by J.P Fleurial at JPL - to be tested in power tile configuration summer 2002



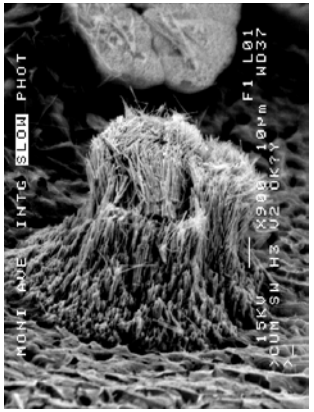
SEM image showing fabricated thermoelectric nanowires. Nanometer -dimensional wires allow for increased efficiency (by over a factor of 2) though the quantum confinement effect.

Power Tile: Major Accomplishments

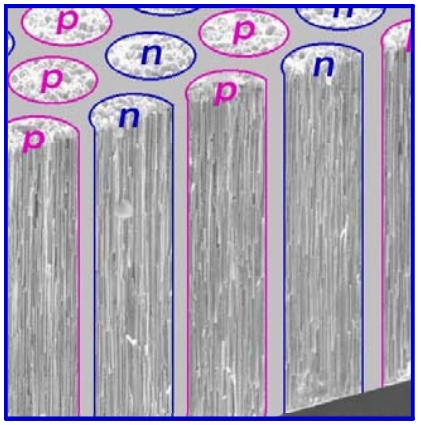
California Institute of Technology

Nanowire-based thermoelectric device

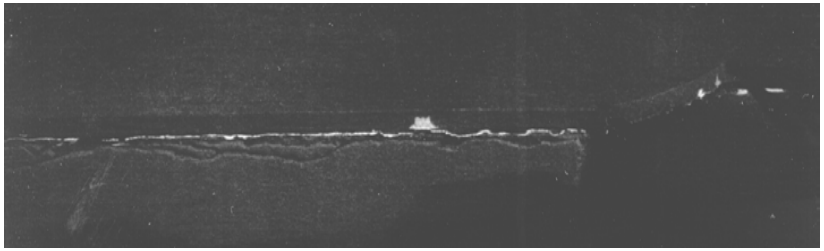
- Development of parylene-based nanowire template patterning process achieved
- Individual nanowire bundles fabricated
- Thermoelectric tests conducted
- Device fabrication under way
- 1000's of legs/cm^2 to provide high voltage device



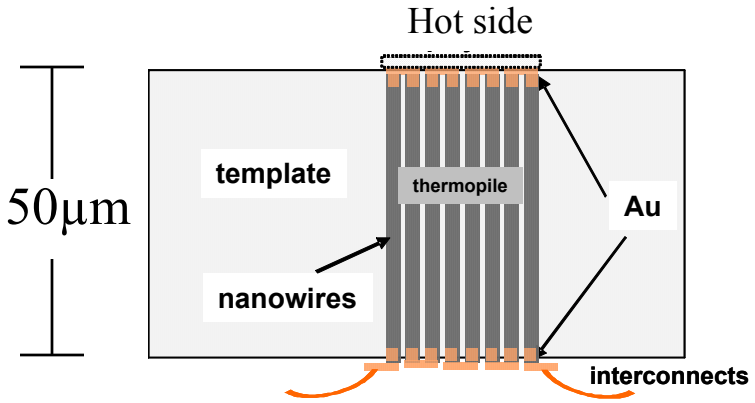
Free-standing nanowire bundle.



Schematic showing bundles of *p*- and *n*- legs in a TE device



Backscatter SEM image showing selected growth of a bundle of Bi_2Te_3 nanowires. Parylene was used as a masking material.

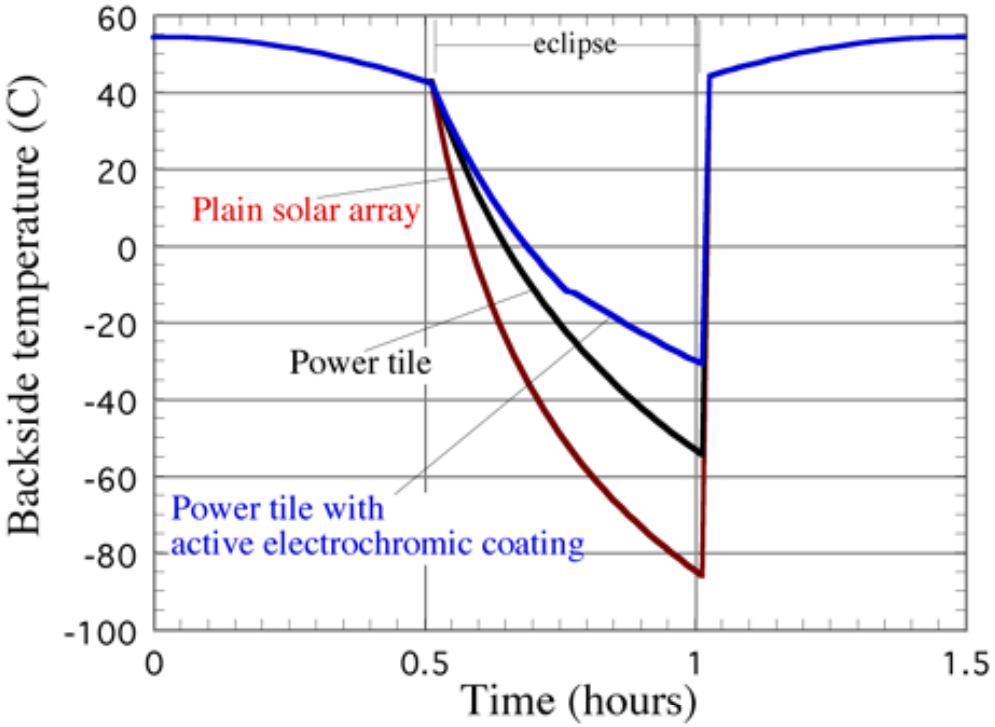


Interconnect scheme for bundles.

task manager: Jay Whitacre

Power Tile: Major Accomplishments

Thermal modeling: Temperature critical to battery/electronics performance



- Electrochromic back coating for thermal management: conducting polymer electrolyte film can have variable emittance: from 0.2 to 0.7 depending on applied field*
- Assume high/low emittance during times of illumination/eclipse

*Chandrasekhar et. al., *Advanced Functional Materials*, 2002, 12, No 2 pg 95

- Low earth orbit operation studied - front side temperature ~90˚C under illumination
- Eclipse temperature extreme less with power tile than in traditional solar array
  - More massive array
- Active electrochromic material keeps battery even warmer.
- Thermoelectric layer could be used to moderate temperature

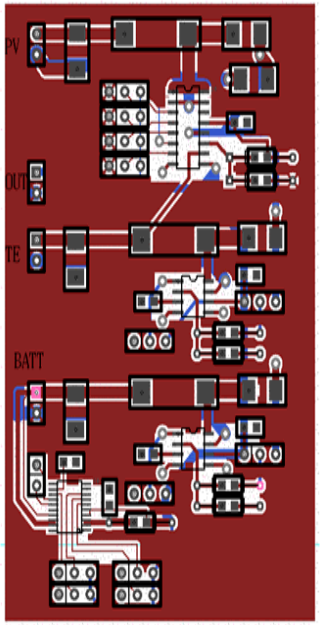
task manager: Jay Whitacre

Power Tile: Major Accomplishments

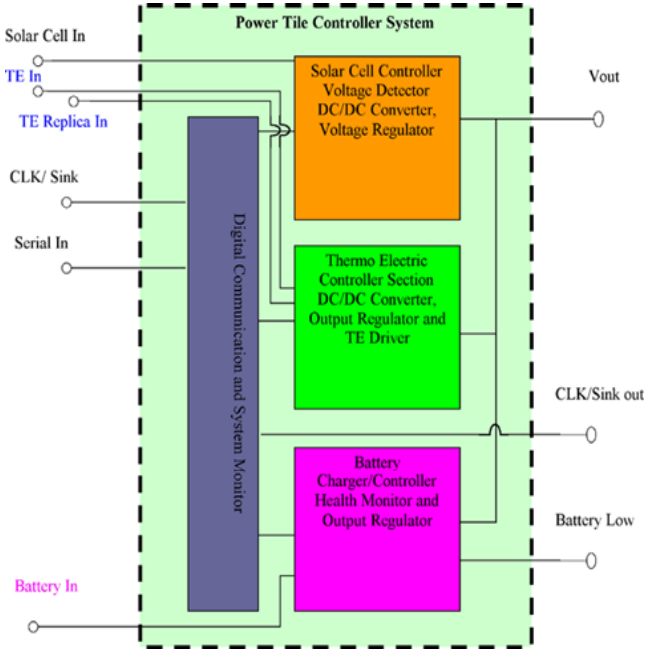
California Institute of Technology

Integrated Power management

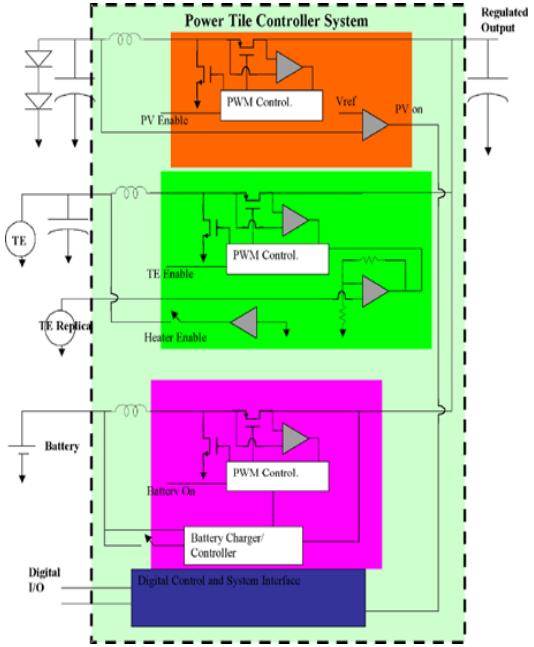
- Received the first version of the electronic controller board for the power tile, debugged the board and submitted it for re-fabrication
- Developed a new concept for electronic biasing the thermoelectric generator to deliver maximum power
- Developed the architectural drawing for a "smart power" power tile controller chip



Layout for controller board



Circuit block diagram

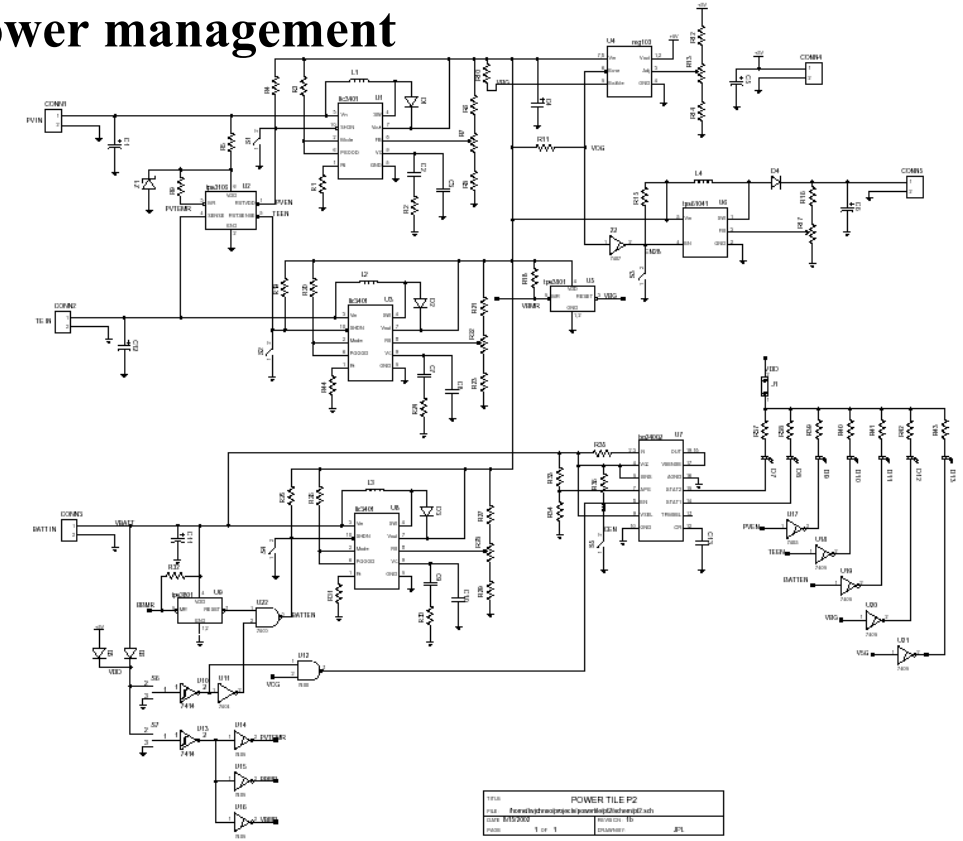


Schematic showing key elements

task manager: Jay Whitacre

Power Tile: Major Accomplishments

Integrated Power management



- The updated version of the electronic controller board for the power tile, is ready for fabrication. In this version synchronous DC-DC converters and autonomous power control circuitry replace the original switching power circuits.
- Developing a complete architectural drawing for a “smart power” power tile controller chip
- Started the design of primitive building block circuits for power tile ASIC and the layout of a test chip that tests these circuits

task manager: Jay Whitacre

Power Tile: Major Accomplishments

California Institute of Technology

Bench top assembly/testing

- Power management circuitry assembled.
- 5 V output to bus
- Power from PV and TE collected, stored in battery
- Full functionality demonstrated

task manager: Jay Whitacre

Power Tile: Major Accomplishments

Prototype assembly/testing

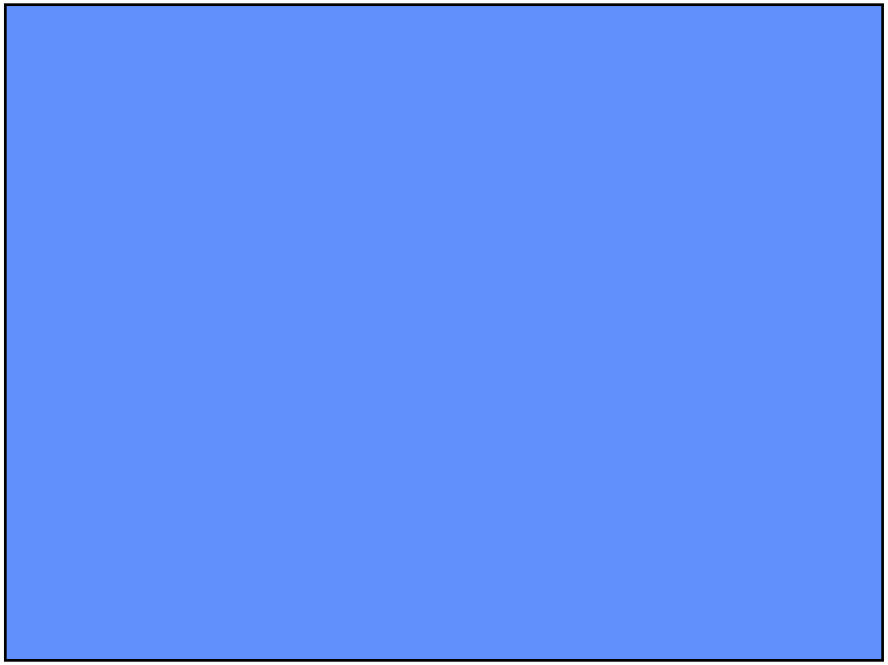
- 3 devices assembled and tested
- Feasibility of thermoelectric generation demonstrated

Prototype device: thickness = 2.1 mm

In X-25 solar simulator

At 0.8 AU:

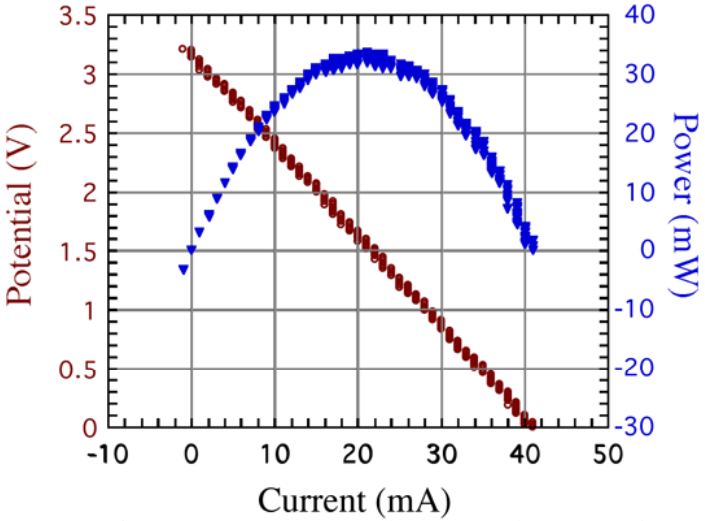
- 2.3 V @ 250 mA from PV cell
- 1.2 V @ 50 mA from TE device
- Backplate kept at 40˚C
- Other test with tile detached from cooling plate also successful
- Charge control circuit allows for efficient DC-DC conversion to 5 V bus, battery charging/discharging
- Efficiency “break even” point surpassed: TE device fully powers charge control electronics - all solar energy available for use.



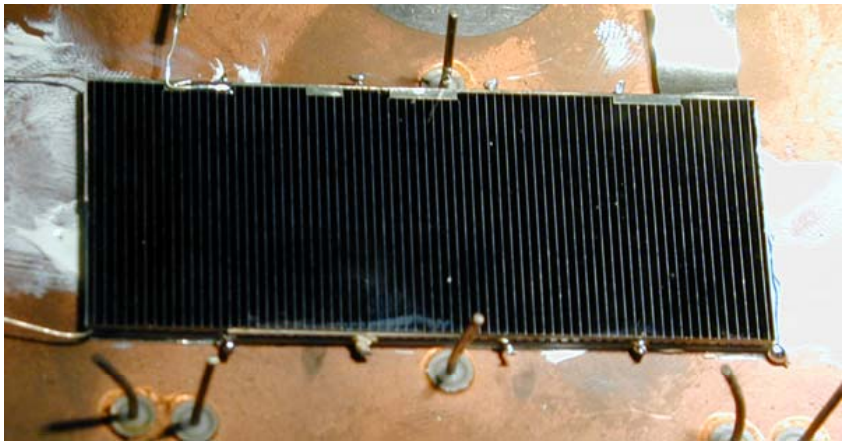
task manager: Jay Whitacre

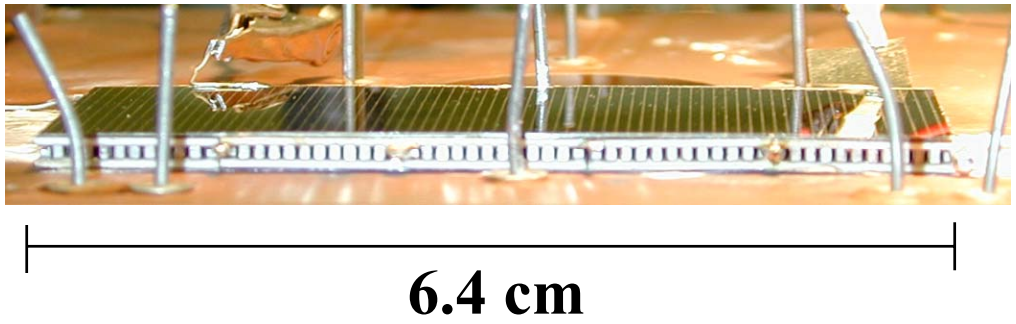
Prototype assembly/testing

- Larger power tile assembled to study scale ability issues.



I-V/I-Power curve for TE device: hot side = 60 ˚C, cold side = 35˚C





6.4 cm

- 1440 leg thermoelectric device
- triple - junction PV cell
- TE device increases overall efficiency by 2% to 5 %

Power Tile: Vision and Goal

California Institute of Technology

Goal: Create modular power harvesting and storage elements with specific power densities that are significantly higher than those currently available.

Value to NASA: Increased specific energy capacity will deliver more power using less massive systems than the state of the art. This technology is possible due to several breakthrough technologies that may be heterogeneously integrated to form the **power tile**:

Technology Development:

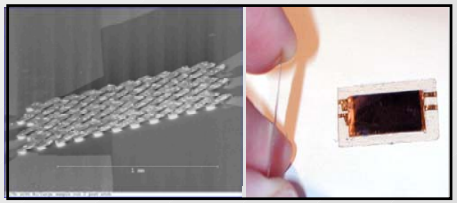
- Solid-state battery system
- Thin-film thermo-electric generator
- Integrated power management and distribution (PMAD)

Capabilities:

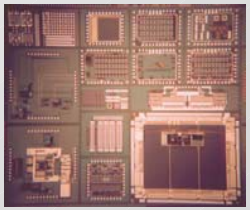
- Energy storage/load leveling
- Energy scavenging/heat pump
- Allow for efficient use/storage of power - provide to main bus

Infusions:

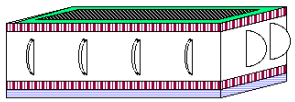
2002 — **JPL microthermo-electric devices/batteries**



2003 — **integrated PMAD**

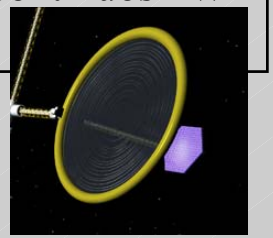


2004 — **High efficiency Power tile/Power box**



housing/power for distributed sensors

2005 — Modular Array system with mass less than 25 kg per continuos kW of power (for GEO)



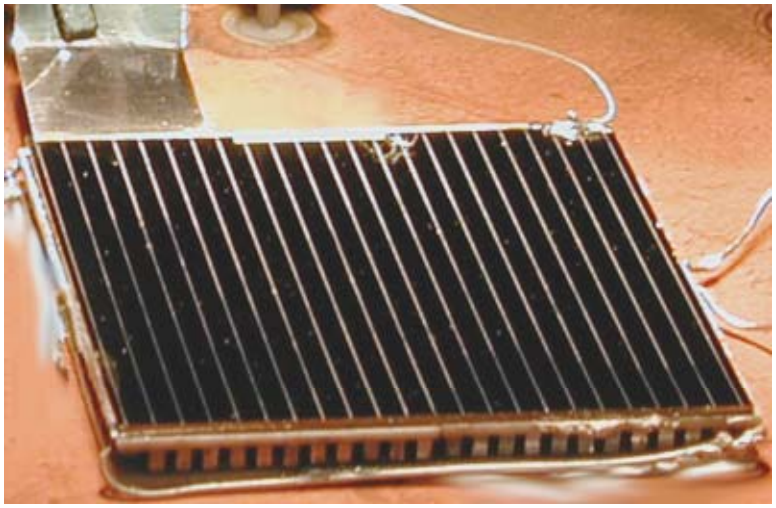
task manager: Jay Whitacre

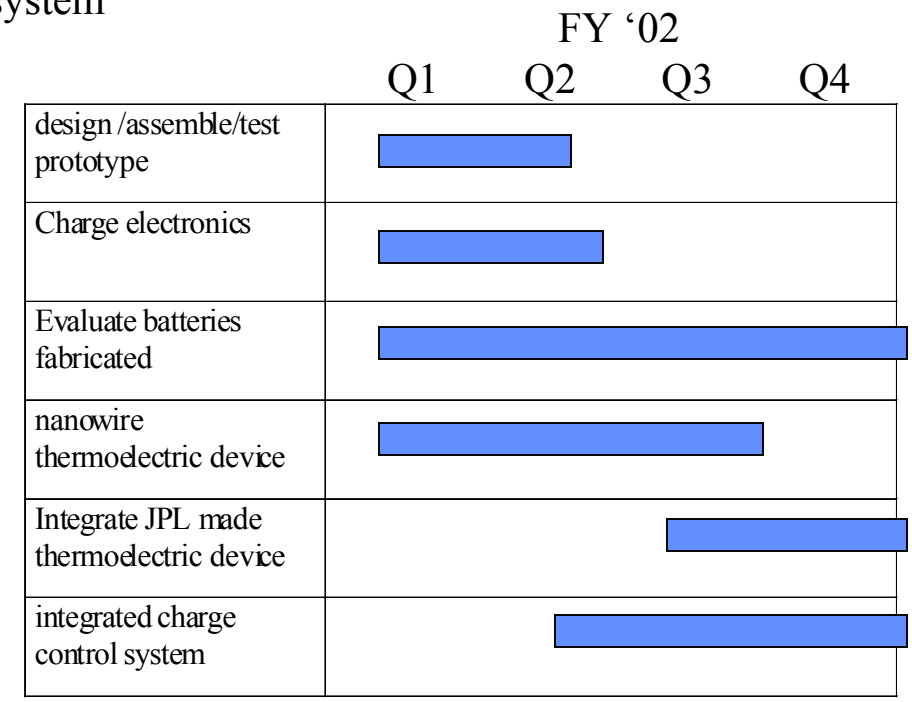
Power Tile: schedule/resources

California Institute of Technology

Task FY'02 Milestones/Products:

- design /assemble/test prototype power tile devices.
- Design/fabricate first generation charge electronics/acquire components
- Evaluate batteries fabricated by industrial partner
- Develop nanowire thermoelectric device
- Integrate JPL made thermoelectric device
- Develop /study ASIC-based integrated charge control system





Resources:

			Planned		
FY'02	FY'03	FY'04	FY'05	FY'06	FY'07
Advanced Concepts Funding:					
$230	$250	$300	$300	$300	$300
Other-Funding:					
$0	$100	$150	$100	$100	$100
FTE's (civil servants and JPL):[Full Time Equivalents]					
0.80	1.00	1.20	1.2	1.2	1.2
EP's (contractors):		[Equivalent Persons]			
0	0	0	0.0	0.0	0

Participants:

JPL, Front Edge Technologies, Univ. of Idaho,

task manager: Jay Whitacre

Planned Accomplishments

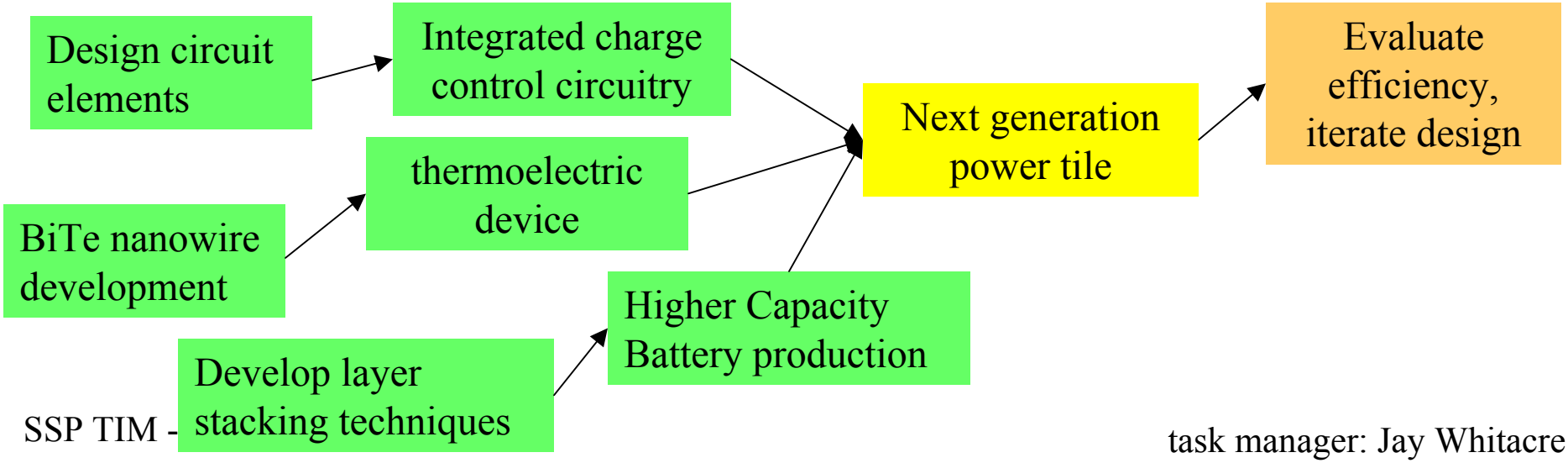
California Institute of Technology

3rd Quarter

- Assemble and test larger area power tile unit (5 x 5 cm)
- Design and submit functional integrated circuit elements for fabrication
- Start to fabricate nanowire-based thermoelectric device
- Obtain 20 mA hour solid-state battery systems

4th Quarter

- Integrate thin film thermoelectric device
- Test integrated integrated charge control elements
- Perform efficiency evaluations



Power Tile: Customer Relevance

Targeted Customer Base

- Space Science
  - Materials development for space applications
- Human Exploration and Development of Space Enterprise
  - Distributed sensor network power
  - Beamed power propulsion concept and development

Co-funding Arrangements

- Current commitments
  - Other NASA Center Participation in SSP
  - Leveraging with university-conducted activities and partnerships
  - NASA JSC HEDS distributed sensor project
- Planned commitments
  - Small business awards
  - Industry leveraging
  - Future NASA funding